IN THE CLAIMS:

We claim:

1. A memory system comprising:

a plurality of T-RAM cells arranged in an array; and

first and second devices connected to the array, wherein each of the plurality of T-RAM cells is fabricated by simultaneously fabricating a first portion of each of the plurality of T-RAM cells and the first devices, and simultaneously fabricating a second portion of each of the plurality of T-RAM cells and the second devices.

2. The memory system according to Claim 1, wherein the first portion of each of the plurality of T-RAM cells is a transfer gate and the second portion of each of the plurality of T-RAM cells is a gated-lateral thyristor storage element.

3. The memory system according to Claim 1, wherein each of the plurality of T-RAM cells has a size of less than or equal to $6F^2$.

4. The memory system according to Claim 1, wherein the plurality of T-RAM cells are fabricated on a semiconductor SOI or bulk wafer.

5. The memory system according to Claim 1, wherein the first devices are n-MOS support devices and the second devices are p-MOS support devices.

6. The memory system according to Claim 1, wherein the first and second devices are interconnected with the plurality of T-RAM cells.

7. The memory system according to Claim 1, wherein each of the plurality of T-RAM cells has a planar cell structure.

8. A T-RAM array comprising:

a plurality of T-RAM cells; and

first and second devices interconnected with the plurality of T-RAM cells, wherein each of the plurality of T-RAM cells is fabricated by simultaneously fabricating a first portion of each of the plurality of T-RAM cells and the first devices, and simultaneously fabricating a second portion of each of the plurality of T-RAM cells and the second devices.

9. The array according to Claim 8, wherein the first portion of each of the plurality of T-RAM cells is a transfer gate and the second portion of each of the plurality of T-RAM cells is a gated-lateral thyristor storage element.

10. The array according to Claim 8, wherein each of the plurality of T-RAM cells has a size of less than or equal to $6F^2$.

11. The array according to Claim 8, wherein the plurality of T-RAM cells and the first and second devices are fabricated on a semiconductor SOI or bulk wafer.

12. The array according to Claim 8, wherein the first devices are n-MOS support devices and the second devices are p-MOS support devices.

13. The array according to Claim 1, wherein each of the plurality of T-RAM cells has a planar cell structure.

14. A method for fabricating a T-RAM array having a plurality of T-RAM cells and first and second devices on a semiconductor wafer, the method comprising the steps of:

simultaneously fabricating a first portion of each of the plurality of T-RAM cells and the first devices; and

simultaneously fabricating a second portion of each of the plurality of T-RAM cells and the second devices.

15. The method according to Claim 14, wherein each of the plurality of T-RAM cells has a size of less than or equal to $6F^2$.

16. The method according to Claim 14, further comprising the step of fabricating the plurality of T-RAM cells and the first and second devices on a semiconductor SOI or bulk wafer.

17. The method according to Claim 14, wherein the first devices are n-MOS support devices and the second devices are p-MOS support devices.

18. The method according to Claim 14, further comprising the step of interconnecting the first and second devices with the plurality of T-RAM cells.

19. The method according to Claim 14, further comprising the step of fabricating each of the plurality of T-RAM cells with a planar cell structure.

20. The method according to Claim 14, further comprising the step of forming gate conductors for each of the plurality of T-RAM cells and for the first and second devices prior to the fabricating steps.

21. The method according to Claim 14, wherein the step of simultaneously fabricating the first portion of each of the plurality of T-RAM cells and the first devices includes the steps of:

providing a mask to conceal the second devices and the second portion of each of the plurality of T-RAM cells;

doping a portion of the semiconductor wafer with a first doping implant; and

doping a portion of the semiconductor wafer in proximity to the portion doped with the first doping implant with a second doping implant.

22. The method according to Claim 21, wherein the first and second doping implants are n-type doping implants.

23. The method according to Claim 21, wherein the step of doping a portion of the semiconductor wafer with a first doping implant includes the step of using an n-type arsenic implant at an energy in the range of 2-15 KeV and a dosage of between $8E14/cm^2$ and $3E15/cm^2$ as the first doping implant.

24. The method according to Claim 21, wherein the step of doping a portion of the semiconductor wafer with a second doping implant includes the step of selecting an n-type boron implant or an n-type BF2 implant as the second doping implant.

25. The method according to Claim 24, wherein if the n-type boron implant is selected as the second doping implant, the method comprises the step of using an n-type boron implant at an energy in the range of 5-30 KeV and a dosage of between $4E13/cm^2$ and $1E14/cm^2$ for doping the portion of the semiconductor wafer; and wherein if the n-type BF2 implant is selected as the second doping implant, the method comprises the step of using an n-type BF2 implant at an energy in the range of 20-120 KeV and a dosage of between $4E13/cm^2$ and $1E14/cm^2$ for doping the portion of the semiconductor wafer.

26. The method according to Claim 14, wherein the step of simultaneously fabricating the second portion of each of the plurality of T-RAM cells while fabricating the second devices includes the steps of:

providing a mask to conceal the first devices and the first portion of each of the plurality of T-RAM cells;

doping a portion of the semiconductor wafer with a first doping implant; and

doping a portion of the semiconductor wafer in proximity to the portion doped with the first doping implant with a second doping implant.

27. The method according to Claim 26, wherein the first and second doping implants are p-type doping implants.

28. The method according to Claim 21, wherein the step of doping a portion of the semiconductor wafer with a first doping implant includes the step of selecting a p-type

boron implant or a p-type BF2 implant as the first doping implant.

29. The method according to Claim 28, wherein if the p-type boron implant is selected as the first doping implant, the method comprises the step of using a p-type boron implant at an energy in the range of 0.5-2 KeV and a dosage of between $2E14/cm^2$ and $8E14/cm^2$ for doping the portion of the semiconductor wafer; and wherein if the p-type BF2 implant is selected as the first doping implant, the method comprises the step of using a p-type BF2 implant at an energy in the range of 3-15 KeV and a dosage of between $2E14/cm^2$ and $8E14/cm^2$ for doping the portion of the semiconductor wafer.

30. The method according to Claim 26, wherein the step of doping a portion of the semiconductor wafer with a second doping implant includes the step of selecting a p-type arsenic implant, a p-type phosphorus implant, or a p-type antimony implant as the second doping implant.

31. The method according to Claim 30, wherein if the p-type arsenic implant is selected as the second doping implant, the method comprises the step of using a p-type arsenic implant at an energy in the range of 50-120 KeV and a dosage of between $2E13/cm^2$ and $8E13/cm^2$ for doping the portion of the semiconductor wafer with the second doping implant; wherein if the p-type phosphorus implant is selected as the second doping implant, the method comprises the step of using a p-type phosphorus implant at an energy in the range of 25-60 KeV and a dosage of between $2E13/cm^2$ and $8E13/cm^2$ for doping the portion of the semiconductor wafer with the second doping implant; and wherein if the p-type antimony implant is selected as the second doping implant, the method comprises the step of using a p-type antimony implant at an energy in the range of 50-150 KeV and a dosage of between $2E13/cm^2$ and $8E13/cm^2$ for doping the portion of the semiconductor wafer with the second doping implant.

32. The method according to Claim 21, further comprising the step of forming a source/drain implant having a halo region in the doped regions of the semiconductor wafer.

33. The method according to Claim 32, wherein the step of forming a source/drain implant comprises the step of using an n-type implant.

34. The method according to Claim 32, wherein the step of forming a source/drain implant includes the step of selecting an n-type arsenic implant or an n-type phosphorus implant for implanting in the doped regions.

35. The method according to Claim 34, wherein if the n-type arsenic implant is selected for implanting in the doped regions, the method comprises the step of using an n-type arsenic implant at an energy in the range of 10-60 KeV and a dosage of between 3E15/cm^2 and 1.5E16/cm^2 for implanting in the doped regions; and wherein if the n-type phosphorus implant is selected for implanting in the doped regions, the method comprises the step of using an n-type phosphorus implant at an energy in the range of 5-30 KeV and a dosage of between 3E15/cm^2 and 1.5E16/cm^2 for implanting in the doped regions.

36. The method according to Claim 32, further comprising the step of forming sidewall spacers in proximity to gate conductors fabricated on the semiconductor wafer prior to the step of forming the source/drain implant.

37. The method according to Claim 26, further comprising the step of forming a source/drain implant having a halo region in the doped regions of the semiconductor wafer.

38. The method according to Claim 37, wherein the step of forming a source/drain implant comprises the step of using a p-type implant.

39. The method according to Claim 38, wherein the step of forming a source/drain implant includes the step of using a p-type boron implant having an energy in the range of 5-20 KeV and a dosage of between 2E15/cm^2 and 5E15/cm^2 for implanting in the doped regions.

40. The method according to Claim 37, further comprising the step of forming sidewall spacers in proximity to gate conductors fabricated on the semiconductor wafer prior to the step of forming the source/drain implant.

41. The method according to Claim 14, further comprising the step of interconnecting the plurality of T-RAM cells and the first and second devices.

42. The method according to Claim 14, wherein the first portion of each of the plurality of T-RAM cells is a transfer gate and the second portion of each of the plurality of T-RAM cells is a gated-lateral thyristor storage element.